Microelectronics
Exercises of Topic 4

ICT Systems Engineering
EPSEM - UPC

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4 Digital integrated circuits

EXERCISE 4.1 Design a CMOS logic gate that implements with the minimum number of transistors the function

$$F = A + \overline{B}C + CD$$

EXERCISE 4.2 Design a logic gate that implements in CMOS technology the XOR (exclusive OR) function, $F = A \bigoplus B$.

EXERCISE 4.3 Given the truth table of function F, which depends on three inputs, A, B and C,

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

answer the following questions:

a) Get a simplified expression for the logic function $F = f(A, B, C)$.

b) Propose the schematic of a CMOS circuit that implements the aforementioned function.

c) Considering that the circuit is loaded with a capacitance much higher than the parasitic capacitances of the transistors, indicate the conditions under which the rise and fall times at the output will be higher (assume that all transistors have the same dimensions).

EXERCISE 4.4 Determine the logic function F performed by the circuit in Figure 1.

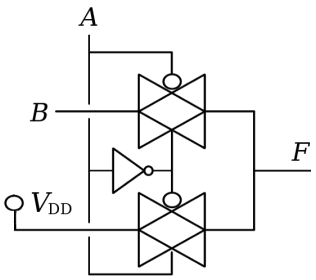

Figure 1

EXERCISE 4.5 One of the problems that some battery-powered electronic circuits exhibit is that the user may accidentally reverse their polarity, submitting the circuit to a reverse voltage able to damage some of its components. A solution to this problem is to incorporate a pass transistor, connected as shown in Figure 2.

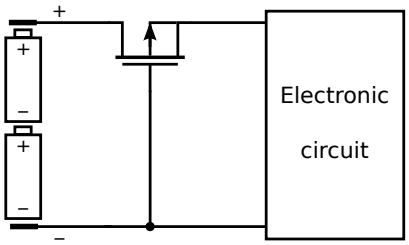

Figure 2

a) Prove that, with a suitable dimensioning, this transistor allows proper circuit operation when the polarity of the batteries is correct and, additionally, it protects the circuit when the polarity is reversed. Assume that the electronic circuit behaves for all purposes as a load resistor.

b) Knowing that the batteries provide a total voltage of 2.4 V and that, when switched on, the circuit draws a current of 100 mA, find the dimensions of the transistor so that the voltage drop between the drain and the source is not greater than 10 mV ($K' = 15\ \mu\text{A/V}^2$, $V_T = -1$ V).

EXERCISE 4.6 Propose an alternative circuit to that in Figure 2 that protects the electronic circuit using an NMOS transistor. Which can be the advantage of using an NMOS transistor instead of a PMOS transistor?

EXERCISE 4.7 Figure 3 shows the symbol and the schematic of a CMOS transmission gate. Knowing that you want to use this gate in a digital circuit with a supply voltage $V_{DD} = 3.3$ V, that the maximum current which is expected to flow through the gate is 10 mA, and that the voltage drop introduced by the device must not exceed 50 mV

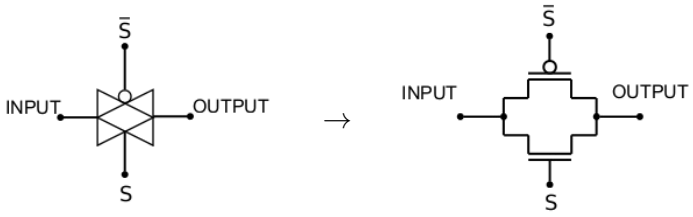

Figure 3

at any of the logic levels to be transferred, determine the appropriate dimensions of the transistors.

Additional data: CMOS technology: 900 nm; NMOS parameters: $K'_N = 50$ µA/V^2, $V_{TN} = 0.5$ V; PMOS parameters: $K'_P = 20$ µA/V^2, $V_{TP} = -0.7$ V.

Exercise 4.8 The diagram in Figure 4 corresponds to that of a single-output CMOS logic gate designed with Magic VLSI Layout Tool.

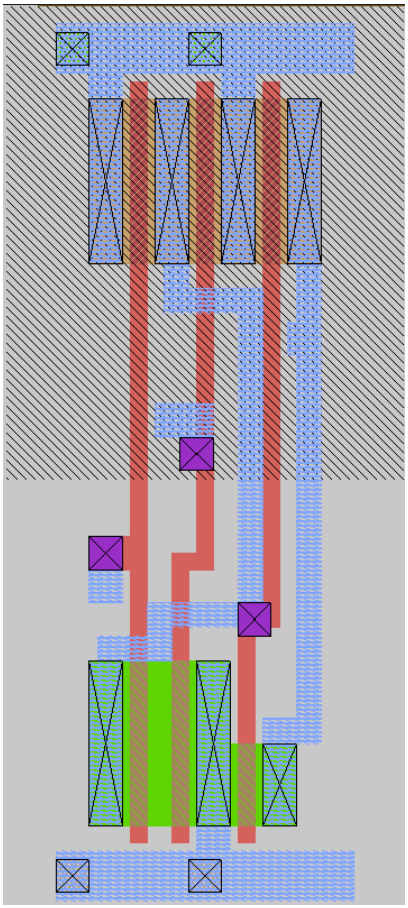

Figure 4

a) From the supplied diagram, plot the gate circuit schematic clearly identifying the inputs and the output.

b) Determine the truth table as well as the boolean expression of the logic function.

EXERCISE 4.9 The diagram in Figure 5 corresponds to that of a CMOS logic gate (*standard cell*) from the 0.35 µm libraries provided by the Oklahoma State University. For efficiency and occupied-area reasons, some of the transistors use a *fingers* layout.

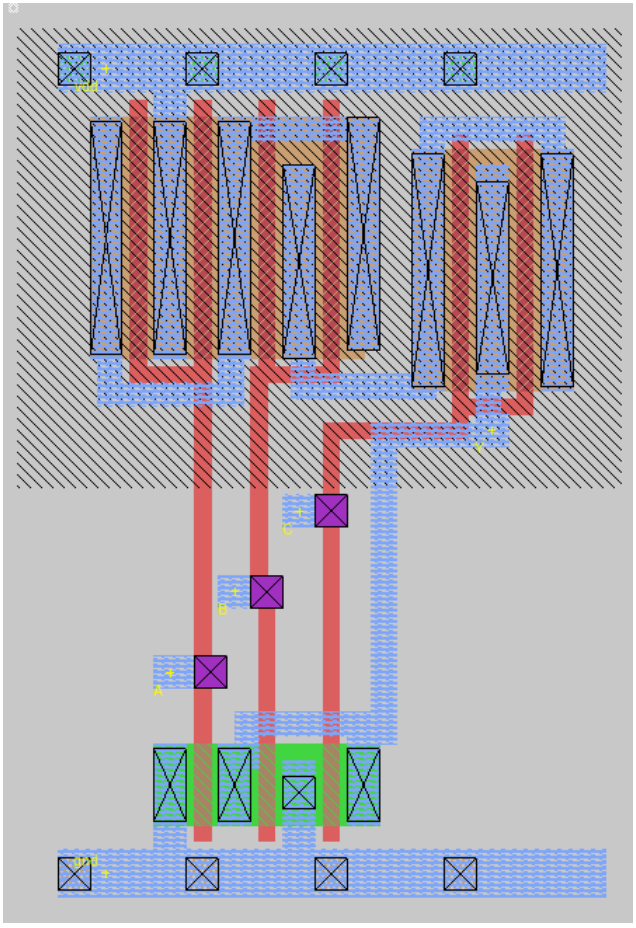

Figure 5

a) From the provided diagram and knowing that the gate has a single output, plot the circuit schematic clearly identifying the inputs and the output.

b) Determine the truth table as well as the boolean expression of the logic function.

EXERCISE 4.10 The website http://opencircuitdesign.com describes the digital synthesis tool Qflow as "*a complete tool chain for synthesizing digital circuits starting from Verilog source and ending in physical layout for a specific target fabrication process*". The site explains that the synthesis process is based on the use of various tools, namely:

- Qrouter: *Detail router*;
- Vhd2vl: *VHDL-to-Verilog translator*;
- Magic: *Final Layout generator/viewer*;
- Yosys: *Verilog parser/synthesis*;
- Graywolf: *Cell and pin placement.*

a) Indicate the order in which each of these programs is called and executed.

b) Explain in some detail the main function that each one performs.

EXERCISE 4.11 Propose a circuit schematic that corresponds to the layout in Figure 6 and identify its functionality.

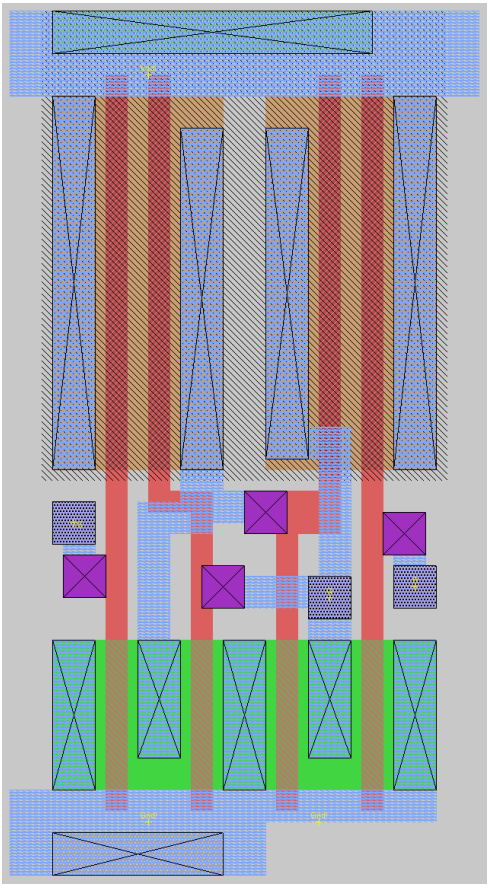

Figure 6